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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/712,218

11/13/2003

Jon Beecroft

SHP-PT080

8480

3624

7590

02/23/2006

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EXAMINER

MASDON, DAVID T

ART UNIT

PAPER NUMBER

2188

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,218	BEECROFT ET AL.	
	Examiner	Art Unit	
	David Masdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 December 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on 13 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>11/13/03 - 12/19/05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) were submitted on 11/13/2003, 6/25/2004 & 12/19/2005. The submissions are in compliance with the provisions of 37 CFR 1.97 and 1.98, except as noted below.

German reference (4,305,860) is being considered only to the extent by applicant's statement of equivalency to US patent 5,696,925.

Drawings

2. The drawings filed on 11-13-2003 have been approved by the examiner.

Specification

3. The disclosure is objected to because of the following informalities: the word 'actioning' needs to be better defined or replaced (page 6, line 16).

Appropriate correction is required.

Claim Objections

4. Claims 7,9 objected to because of the following informalities:

As per claim 7, the word 'actioning' (line 20) needs to be better defined or replaced.

As per claim 9, the word 'search' (line 4) needs to be replaced with 'searched'.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2, 4,6-11,13,15 are rejected under 35 U.S.C 103 (a) as being unpatentable over Forin (US 6,321,276) in view of Macdonald et al (US 5,696,927) and in further view of Chesson et al (US 6,223,270).

As per claims 1-2, Forin discloses a network system with network interface adapters that incorporate translation between virtual addresses and physical addresses. These network interface adapters also include memory management units and memory with page tables. (column 7, lines 4-20) Forin does not disclose compressing virtual addresses or a mapping table which is ordered with respect to compressed versions of the virtual address. However, MacDonald et al discloses a memory page system with compressed entries that maps virtual addresses to the respective physical addresses. (column 3, lines 16-44) Macdonald et al also discloses compression algorithms. (column 13, lines 52-61)

Forin and Macdonald et al are analogous art because they are from the same field of endeavor, namely virtual memory addresses. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the virtual

address compression of Macdonald et al into the system of Forin. The motivation for doing so would have been to reduce storage requirements for data. (MacDonald et al; column 2, lines 65-67)

Forin and Macdonald et al do not disclose expressly 64 bit virtual addresses. However, Chesson et al discloses a 64-bit virtual address. (column 6, lines 62-64)

Forin, MacDonald et al, and Chesson et al are analogous art because they are from the same field of endeavor, namely virtual memory addresses. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the 64-bit virtual address of Chesson et al into the system of Forin and Macdonald et al. The motivation for doing so would have been to increase system efficiency and prevent memory addresses from intersecting. (Chesson et al; column 6, lines 60-67; column 7, lines 1-11)

As per claim 2, Macdonald et al discloses translation lookaside buffers used for mapping. (column 3, lines 31-34)

As per claim 4, MacDonald et al discloses a computer network as claimed in claim 1, wherein each entry of the mapping table of the memory management unit includes two tags representative of two virtual addresses. [(each entry contains base address and table information) column 1, lines 40-66]

As per claim 6, Forin discloses a computer network as claimed in claim 1, wherein each entry of the mapping table further includes a chain pointer, which is used to identify alternate entries in the mapping table for different virtual addresses having identical compressed virtual addresses. [(pointer to descriptor specified by virtual address) column 17, lines 1-14)

Claims 7, 10 rejected with the same rationale of claim 1. MacDonald et al discloses pages with compressed entries that map virtual addresses to respective physical memory. (column 3, lines 21-42) Macdonald et al also discloses an address mapping hierarchy used to access a particular physical address. (column 6, lines 15-41)

Claims 8,11 are rejected with the same rationale of claim 2. MacDonald et al discloses an compression/decompression engine that traverses compressed page mapping hierarchy to the referenced compressed page table entry. (column 11, lines 55-67)

As per claim 9, MacDonald discloses a compression/decompression engine that handles mapping pages with different sizes. (column 11, lines 8-21)

Claim 13 is rejected with the same rationale of claim 4.

Claim 15 is rejected with the same rationale of claim 6.

6. Claims 3,12 rejected under 35 U.S.C. 103(a) as being unpatentable over Forin (US 6,321,276), Macdonald et al (US 5,696,927), and Chesson et al (US 6,223,270) as applied to claims 1-2, 4-15 above, and further in view of Burns et al (US 2002/0199089).

Forin, MacDonald et al, and Chesson et al fail to expressly disclose a computer network as claimed in claim 2, further comprising a thread processor and a microcode processor, wherein one translation lookaside buffer of the memory management unit is dedicated to the thread processor and the other translation lookaside buffer is dedicated to the microcode processor of the network interface. Burns et al discloses a thread processor system with a microcode processor and a buffer for the system. [(buffers for threads in processor system) paragraphs 0004, 0005, 0019, 0026]

Forin, MacDonald et al, Chesson et al and Burns et al are analogous art because they are from the same field of endeavor, namely processors and memory. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the two processors and buffers of Burns et al into the system of Forin, MacDonald et al, Chesson et al. The motivation for doing so would have been to help resolve instruction starvation. (Burns et al; page 1, paragraphs 0001-0006)

Claim 12 is rejected with the same rationale of claim 3.

7. Claims 5,14 rejected under 35 U.S.C. 103(a) as being unpatentable over Forin (US 6,321,276), Macdonald et al (US 5,696,927), and Chesson et al (US 6,223,270) as applied to claims 1-2, 4-15 above, and further in view of Matick et al (US 4,577,293).

Forin, MacDonald et al, and Chesson et al fail to expressly disclose a computer network as claimed in claim 1, wherein each entry of the mapping table of the memory management unit includes two tags representative of two virtual addresses. Matick et al discloses tags in the cache directory that are real memory addresses. (column 5, lines 30-40)

Forin, MacDonald et al, Chesson et al and Matick et al are analogous art because they are from the same field of endeavor, namely cache. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate tags associated with addresses of Matick et al into the system of Forin, MacDonald et al, Chesson et al. The motivation for doing so would have been to help optimize cache usage in systems. (Burns et al; column 1, lines 19-60)

Claim 14 is rejected with the same rationale of claim 5.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

US 2003/0225992 – Venkatrao et al – METHOD AND SYSTEM OF ADDRESS TAGS

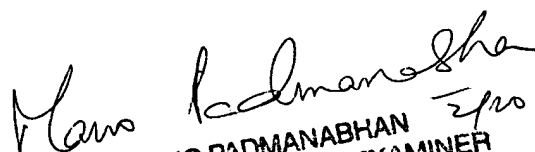
US 2002/0073298 – Geiger et al – SYSTEM AND METHOD FOR MANAGING
COMPRESSION

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Masdon whose telephone number is (571)272-6815. The examiner can normally be reached on Monday - Friday, 7am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DM
Tuesday, February 14, 2006


MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
2/14/06